AMENDMENTS TO THE CLAIMS

1. **(Original)** A signal receiver for receiving a differential input signal pair through an external differential input terminal pair, comprising:

a positive feedback differential amplifier having a differential input terminal pair and a differential output terminal pair;

a coupling circuit, coupled to the external differential input terminal pair, the differential input terminal pair and the differential output terminal pair, for coupling the differential input signal pair on the external differential input terminal pair to the differential input terminal pair; and

a pre-charger for pre-charging the differential input terminal pair to a predetermined voltage level;

wherein the differential input terminal pair is coupled to the external differential input terminal pair before a first time point, the differential input signal pair enters into the differential input terminal pair of the positive feedback differential amplifier via the coupling circuit after the first time point, and the positive feedback differential amplifier is activated to amplify the entered differential input signal pair and outputs to the differential output terminal pair at a second time point a predetermined period after the first time point.

2. **(Original)** The signal receiver as claimed in claim 1, wherein the coupling circuit includes a first coupling circuit and a second coupling circuit, the first coupling circuit comprising:

a first transistor of a first type; and

a second transistor of a second type, wherein the gates of the first transistor and the second transistor are coupled to a first terminal of the differential output terminal pair, sources of the first transistor and the second transistor are coupled to a first terminal of the differential input terminal pair, and a drain of the first transistor serves as a first terminal of the external differential input terminal pair;

and the second coupling circuit comprising:

a third transistor of the first type; and

a fourth transistor of the second type, wherein gates of the third transistor and the fourth transistor are coupled together to a second terminal of the differential output terminal pair, sources of the third transistor and fourth transistor are coupled together to a second terminal of the differential input pair, and a drain of the third transistor serves as a second terminal of the external differential input terminal pair.

3. **(Original)** The signal receiver as claimed in claim 2, wherein the first type transistors are PMOS transistors, the second type transistors are NMOS transistors, and drains of the second transistor and the fourth transistor are connected to the ground.

4. **(Original)** The signal receiver as claimed in claim 2, wherein the first type transistors are PMOS transistors, the second type transistors are NMOS transistors, and drains of the second transistor and the fourth transistor are connected to a high voltage.

5. **(Original)** The signal receiver as claimed in claim 1, wherein the coupling circuit includes a first coupling circuit and a second coupling circuit, the first coupling circuit comprising:

a first capacitor having a first end coupled to a first terminal of the external differential input terminal pair; and

a fifth transistor having a gate connected to a first terminal of the differential output terminal pair, and a drain connected to a second end of the first capacitor and a first terminal of the differential input terminal pair;

and the second coupling circuit comprising:

a second capacitor having a first end coupled to a second terminal of the external differential input terminal pair; and

a sixth transistor having a gate connected to a second terminal of the differential output terminal pair, and a drain connected to a second end of the second capacitor and a second terminal of the differential input terminal pair.

6. **(Original)** The signal receiver as claimed in claim 5, wherein the fifth transistor and the sixth transistor are NMOS transistors having sources connected to the ground.

7. **(Original)** The signal receiver as claimed in claim 5, wherein the fifth transistor and the sixth transistor are PMOS transistors, having their sources connected to a high voltage.

8. **(Original)** The signal receiver as claimed in claim 1, wherein the pre-charger comprises:

a first local control transistor having a gate connected to a first control signal for pre-charging a first terminal of the differential input terminal pair to the predetermined voltage level before the first time point, the first local control transistor being turned off after the first time point; and

a second local control transistor having a gate connected to the first control signal for pre-charging a second terminal of the differential input terminal pair to the predetermined voltage level before the first time point, the second local control transistor being turned off after the first time point;

wherein the external differential input terminal pair are pre-charged to the predetermined voltage level before the first time point and the positive feedback differential amplifier is controlled with a second control signal for defining the second time point.

9. **(Original)** The signal receiver as claimed in claim 1, wherein the pre-charger comprises:

a third local control transistor having a gate connected to a second control signal, and a source and a drain connected to the differential output terminal pair, wherein the second control signal is used for defining the second time point.

10. **(Original)** A signal receiver for receiving an independent input signal via an external input terminal, comprising:

a positive feedback differential amplifier having a differential input terminal pair and a differential output terminal pair;

a coupling circuit, coupled to the external input terminal, the differential input terminal pair and the differential output terminal pair, for coupling the independent input signal on the external input terminal to the differential input terminal pair; and

a pre-charger for pre-charging the differential input terminal pair to a predetermined voltage level;

wherein one of the differential input terminal pair is coupled to the external input terminal before a first time point, wherein

the independent input signal enters the differential input terminal pair of the positive feedback differential amplifier via the coupling circuit after the first time point, and the positive feedback differential amplifier is activated to amplify the entered independent input signal and outputs to the differential output terminal pair at a second time point a predetermined period after the first time point.

11. **(Original)** The signal receiver as claimed in claim 10, wherein the coupling circuit includes a first coupling circuit and a second coupling circuit, the first coupling circuit comprising:

a first capacitor having a first end coupled to the external input terminal; and

a first transistor having a gate connected to a first terminal of the differential output terminal pair, and a drain connected to a second end of the first capacitor and a first terminal of the differential input terminal pair;

and the second coupling circuit comprising:

a second capacitor having a first end connected to a fixed voltage level; and

a second transistor having a gate connected to a second terminal of the differential output terminal pair, and a drain connected to a second end of the second capacitor and a second terminal of the differential input terminal pair.

12. **(Original)** The signal receiver as claimed in claim 11, wherein the first transistor and the second transistor are NMOS transistors having sources connected to the ground.

13. **(Original)** The signal receiver as claimed in claim 11, wherein the first transistor and the second transistor are PMOS transistors having sources connected to a high voltage.

14. **(Original)** The signal receiver as claimed in claim 10, wherein the pre-charger comprises:

a first local control transistor having a gate connected to a first control signal for pre-charging a first terminal of the differential input terminal pair to the predetermined voltage level before the first time point, the first local control transistor being turned off after the first time point; and

a second local control transistor having a gate connected to the first control signal for pre-charging a second terminal of the differential input terminal pair to the predetermined voltage level before the first time point, the second local control transistor being turned off after the first time point;

wherein the external input terminal is pre-charged to the predetermined voltage level via the coupling circuit before the first time point and the positive feedback differential amplifier is controlled with a second control signal for defining the second time point.

15. **(Currently Amended)** A signal transmitter for transmitting a differential input signal pair to a transmission line, comprising:

~~via~~ an external differential output terminal connecting to the transmission line;~~, comprising:~~ and

a control circuit, controlled by a first control signal for defining a first time point, for pre-charging the transmission line to a predetermined voltage level via the external differential output terminal before the first time point, and transmitting the differential input signal pair to the transmission line after the first time point~~.~~, wherein the control circuit includes:

a first logic gate having an input terminal pair coupled to the first control signal and a first signal of the differential input signal pair, and an output terminal coupled to a first

terminal of the external differential output terminal, for pre-charging a first path of the transmission line to the predetermined voltage level via the first terminal of the external differential output terminal before the first time point, and substantially transmitting the first signal of the differential input signal pair to the first path of the transmission line after the first time point; and

a second logic gate having an input terminal pair coupled to the first control signal and a second signal of the differential input signal pair, and an output terminal coupled to a second terminal of the external differential output terminal, for pre-charging a second path of the transmission line to the predetermined voltage level via the second terminal of the external differential output terminal before the first time point, and substantially transmitting the second signal of the differential input signal pair to the second path of the transmission line after the first time point.

16. **(Original)** The signal transmitter as claimed in claim 15, wherein the control circuit is a differential circuit coupled to the external differential output terminal and controlled by the first control signal, wherein the differential circuit has a dynamic load controlled by the first control signal for pre-charging the transmission line to the predetermined voltage level.

17. **(Original)** The signal transmitter as claimed in claim 15, wherein the control circuit is a differential circuit coupled to the external differential output terminal and controlled by the first control signal, wherein the differential circuit has a fixed load for pre-charging the transmission line to the predetermined voltage level.

18. **(Cancelled)**

19. **(Currently Amended)** The signal transmitter as claimed in claim ~~18~~15, wherein the first logic gate and the second logic gate are NAND gates.

20. **(Currently Amended)** The signal transmitter as claimed in claim ~~18~~15, wherein the first logic gate and the second logic gate are NOR gates.

21. **(Original)** The signal transmitter as claimed in claim 15, wherein the control circuit substantially cuts off the interconnection between the differential input signal pair and the transmission line within a predetermined period after the first time point.

22. **(Original)** The signal transmitter as claimed in claim 21, wherein the control circuit includes:

a first differential circuit having an input terminal pair connected to the first control signal and the external differential output terminal, and an output terminal pair for outputting a feedback signal pair; and

a second differential circuit having an input terminal pair connected to the first control signal, the differential input signal pair and feedback signal pair, and an output terminal pair connected to the external differential input terminal.

23. **(Original)** The signal transmitter as claimed in claim 21, wherein the control circuit comprises:

a first logic gate having an input terminal connected to the first control signal, a first signal of the differential input signal pair and a first feedback signal, and an output terminal

connected to a first terminal of the external differential output terminal;

a second logic gate having an input terminal connected to the first control signal, a second signal of the differential input signal pair and a second feedback signal, and an output terminal connected to a second terminal of the external differential output terminal;

a third logic gate having an input terminal connected to the first control signal and the first terminal of the external differential output terminal, and an output terminal for outputting the first feedback signal; and

a fourth logic gate having an input terminal connected to the first control signal and the second terminal of the external differential output terminal, and an output terminal for outputting the second feedback signal.

24. **(Original)** The signal transmitter as claimed in claim 23, wherein the first logic gate, the second logic gate, the third logic gate and the fourth logic gate are NAND gates.

25. **(Original)** A signal transmission system, mounted into a chip and having a signal transmitter and a signal receiver connected with each other by a transmission line, wherein the signal transmitter transmits a differential input signal pair to the transmission line via an external differential output terminal pair and the signal receiver receives the differential input signal pair via the external differential input terminal pair, the signal transmitter comprising:

a control circuit, controlled by a first control signal for defining a first time point for pre-charging the transmission line to a predetermined voltage level via the external differential output terminal pair before the first time point, and substantially

transmitting the differential input signal pair to the transmission line after the first time point;

and the signal receiver comprising:

a positive feedback differential amplifier having a differential input terminal pair and a differential output terminal pair;

a coupling circuit, coupled to the external differential input terminal pair, the differential input terminal pair and the differential output terminal pair, for coupling the differential input signal pair on the external differential input terminal pair to the differential input terminal pair; and

a pre-charger for pre-charging the differential input terminal pair to the predetermined voltage level;

wherein the differential input terminal pair is coupled to the external differential input terminal pair before the first time point, wherein the differential input signal pair enters the differential input terminal pair of the positive feedback differential amplifier via the coupling circuit after the first time point, and the positive feedback differential amplifier is activated to amplify the entered differential input signal pair and outputs to the differential output terminal pair at the second time point a predetermined period after the first time point.

26. **(Original)** The signal transmission system as claimed in claim 25, wherein the control circuit substantially cuts off the interconnection between the differential input signal pair and the transmission line within a predetermined period after the first time point.